Electronic Version

Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1. A charge pump circuit comprising a plurality of driving units cascaded in series, each driving unit comprising:

an input port;

an output port;

a first node;

a second node;

a first capacitor electrically connected to the first node;

a second capacitor electrically connected to the output port;

a first transistor comprising:

a substrate electrically connected to the second node;

a gate electrically connected to the output port;

a drain electrically connected to the input port; and

a source electrically connected to the first node;

a second transistor comprising:

a substrate electrically connected to the second node;

a gate electrically connected to the first node;

a drain electrically connected to the input port; and

a source electrically connected to the output port;

a third transistor comprising:

a substrate electrically connected to a first predeter-

mined voltage;

a gate;

a source electrically connected to the second node; and

a drain electrically connected to the output port; and

a fourth transistor comprising:

a substrate electrically connected to a second predetermined voltage;

a gate;

a source electrically connected to the second node; and

a drain electrically connected to the input port;

wherein the gate of the fourth transistor within one driving unit is electrically connected to the gate of the third transistor within previous adjacent driving unit.

[c2] 2. The charge pump circuit of claim 1 wherein the first, second, third, and fourth transistors are p-channel metal-oxide semiconductor (PMOS) transistors.

[c3] 3. The charge pump circuit of claim 1 wherein the first, second, third, and fourth transistors are n-channel metal-oxide semiconductor (NMOS) transistors.

[c4] 4. The charge pump circuit of claim 1 wherein each of the first, second, third, fourth transistors comprises a triple well structure.

[c5] 5. The charge pump circuit of claim 1 further comprising

an input unit connected to a beginning of the driving units cascaded in series, the input unit comprising:

an input port;

an output port electrically connected to the input port of the driving unit which is positioned in the beginning of the driving units cascaded in series;

a first node;

a second node;

a first capacitor electrically connected to the first node;

a second capacitor electrically connected to the output port;

a first transistor comprising:

a substrate electrically connected to a third predetermined voltage;

a gate electrically connected to the output port;

a drain electrically connected to the input port; and

a source electrically connected to the first node;

a second transistor comprising:

a substrate electrically connected to the second node;

a gate electrically connected to the first node;

a drain electrically connected to the input port; and

a source electrically connected to the output port; and

a third transistor comprising:

a substrate electrically connected to a fourth predetermined voltage;

a gate electrically connected to the first node and the

gate of the fourth transistor of the driving unit positioned in the beginning of the driving units cascaded in series;

a source electrically connected to the second node; and

a drain electrically connected to the output port.

[c6] 6. The charge pump circuit of claim 1 further comprising an output unit connected to a last of the driving units cascaded in series, the output unit comprising:

an input port electrically connected to the output port of the last of the driving units cascaded in series;

an output port;

a first node;

a first capacitor electrically connected to the input port;

a second capacitor electrically connected to the output port;

a first transistor comprising:

a substrate electrically connected to the first node;

a gate electrically connected to the input port;

a drain electrically connected to the input port; and

a source electrically connected to the output port; and

a second transistor comprising:

a substrate electrically connected to a fifth predetermined voltage;

a gate electrically connected to the gate of the third transistor of the last of the driving units cascaded in se-

ries;

a source electrically connected to the substrate of the first transistor; and

a drain electrically connected to the input port.